WHAT IS CLAIMED IS:

1. A trenched DMOS device formed atop an N+ silicon substrate with an N epitaxial layer thereon including a device region and a bus region neighboring the device region, the device region comprising:

a P substrate, formed in the epitaxial layer and extending to a top surface thereof, a plurality of DMOS trenches extending downward through the P substrate from a top surface thereof;

a gate oxide layer formed in the DMOS trenches and extending to cover the top surface of the P substrate;

a plurality of polysilicon gates formed in the DMOS trenches;

a plurality of N+ source regions formed in the P substrate adjacent the DMOS trenches;

a plurality of P+ diffused regions formed in the P substrate and each being interposed between two of the N+ source regions;

a first isolation layer formed over the P substrate to cover the polysilicon gate electrodes; and

a source metal contact layer formed on the first isolation layer and connecting to the N+ source regions and the P+ diffused regions;

and the bus region comprising:

a P substrate, formed in the epitaxial layer and extending to a top surface of the epitaxial layer, a field oxide layer being formed on the P substrate and a bus trench extending down from a top surface of the field oxide layer to a lower portion of the P substrate;

a gate oxide layer formed in the bus trench and extending to cover a top surface of the P substrate;

a polysilicon bus formed in the bus trench and having a top surface disposed at a lower level than the top surface of the field oxide layer;

a second isolation layer covering the field oxide layer and having an opening to expose the polysilicon bus; and

a metal line formed atop the polysilicon bus.

2. The trenched DMOS device of claim 1, wherein the P substrate of the device region and the P substrate of the bus region are formed by ion implantation simultaneously.

3. The trenched DMOS device of claim 1, wherein the gate oxide layer of the device region and the gate oxide layer of the bus region are formed simultaneously.

4. The trenched DMOS device of claim 1, wherein the polysilicon gate and the polysilicon bus are formed by depositing a polysilicon layer in the DMOS trenches and the bus trench and using the gate oxide layers as etch stop layers to etch the polysilicon layer.

5. The trenched DMOS device of claim 1, wherein the plurality of N+ source regions are formed in the P substrate on opposite sides of each of the DMOS trenches.

6. A semiconductor device set which comprises at least two types of devices, each of the two types of devices having a trench feature;

wherein the first device comprises a gate oxide formed in the trench feature, a polysilicon layer formed on the gate oxide in the trench features, a first isolation layer formed on the polysilicon layer and having an opening, and a metal layer formed on the first isolation layer and filling the opening of the first isolation layer; and

wherein the second device comprises a dielectric layer formed adjacent an opening at a top of the trench feature on opposite sides of the trench feature, a gate oxide formed in the trench feature and over the dielectric layer, a polysilicon layer formed on the gate oxide in the trench feature including a space near the top of the trench feature with the dielectric layer disposed on opposite sides thereof, a second isolation layer formed on the dielectric layer, and a metal layer formed on the polysilicon layer.

7. The semiconductor device set of claim 6, wherein the at least two types of devices are formed on a silicon substrate.

8. The semiconductor device set of claim 7, wherein the silicon substrate has an epitaxial layer formed thereon.

9. The semiconductor device set of claim 8, wherein the epitaxial layer has a P substrate thereon.

10. The semiconductor device set of claim 9, wherein each trench feature extends through the P substrate to an area below a top surface of the epitaxial layer.

11. The semiconductor device of claim 9, wherein a plurality of N source regions and a plurality of P regions are formed in the P substrate.

12. The semiconductor device of claim 11, wherein at least two of the N source regions formed in the P substrate are disposed adjacent to and on opposites sides of one of the first devices, and wherein at least one of the P regions formed in the P substrate is disposed between two adjacent N source regions.

13. The semiconductor device of claim 8, wherein the epitaxial layer is an N epitaxial layer.

14. The semiconductor device of claim 7, wherein the silicon substrate is an N substrate.

15. The semiconductor device of claim 6 wherein the dielectric layer in the second device comprises a field oxide layer.

16. A method of forming a trenched DMOS device, the method comprising:

providing an N+ silicon substrate with an N epitaxial layer thereon, and a P substrate in the N epitaxial layer extending to a top surface thereof;

forming in a device region a plurality of DMOS trenches extending downward through the P substrate from a top surface thereof, and in a bus region a field oxide layer on the P substrate and a bus trench extending down from a top surface of the field oxide layer to a lower portion of the P substrate;

forming a gate oxide layer in the DMOS trenches which extends to cover the top surface of the P substrate adjacent the DMOS trenches, and a gate oxide layer in the bus trench which extends to cover the top surface of the P substrate adjacent the bus trench;

forming a plurality of polysilicon gates in the DMOS trenches, and a polysilicon bus in the bus trench, the polysilicon bus having a top surface disposed at a lower level than the top surface of the field oxide layer;

forming a plurality of N+ source regions in the P substrate adjacent the DMOS trenches;

forming a plurality of P+ diffused regions in the P substrate, each of the P+ diffused regions being interposed between two of the N+ source regions;

forming a first isolation layer over the P substrate to cover the polysilicon gates, and a second isolation layer to cover the field oxide layer, the second isolation layer having an opening to expose the polysilicon bus; and

forming a source metal contact layer on the first isolation layer, and a metal line atop the polysilicon bus, the source metal contact layer connecting to the N+ source regions and the P+ diffused regions.

17. The method of claim 16, wherein the P substrate of the device region and the P substrate of the bus region are formed by ion implantation simultaneously.

18. The method of claim 16, wherein the gate oxide layer of the device region and the gate oxide layer of the bus region are formed simultaneously.

19. The method of claim 16, wherein the polysilicon gate and the polysilicon bus are formed by depositing a polysilicon layer in the DMOS trenches and the bus trench and using the gate oxide layers as etch stop layers to etch the polysilicon layer.

20. The method of claim 16, wherein the plurality of N+ source regions are formed in the P substrate on opposite sides of each of the DMOS trenches.